REMARKS

Claims 1-20 have been presented for examination in the above-identified U.S. Patent Application.

Claims 1-20 have been rejected in Office Action dated November 26, 2004, the Office Action imposing a final rejection on all claims.

Claims 1, 8, and 12 have been amended by this Amendment B.

Claim 2 has been cancelled by this Amendment B.

Claim 21 has been added by this Amendment B.

Claims 1 and 3-21 are in the Application and reconsideration of the Application is hereby respectfully requested.

Referring to Paragraph No. 6 of Page 2 and continuing through Paragraph 11 on Page 7 of Office Action dated November 26, 2004, Claims 1-20 have been provisionally rejected under the doctrine of obviousness double patenting. As indicated by Examiner, responses to the double patenting rejection, such as the terminal disclaimer, are available. However, because these rejections are provisional, at present, i.e., no Claim having been allowed in either the present Application or the referenced Applications, Applicant prefers to place this matter in abeyance pending the outcome of the prosecution of the Application and/or the references.

However, Applicant appreciates the detail provided by Examiner.

Referring to Paragraph Nos. 10-20, Claims 1-20 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. 5,845,153 issued in the name of Sun et al (hereinafter referred to as Sun). Before directly addressing the rejection, the invention disclosed by the Application will be summarized. The Utopia protocol implements a procedure for transferring data between data processing machines. A Utopia-protocol interface is needed to interface between the data processing systems. In the present invention, the Utopia interface interfaces with the direct memory access unit of the processor. The signals defined by the Utopia protocol are given in Table 1 on Page 6 and 7 of the Specification. For particular implementations using the Utopia protocol, other signals can be added. For example, the WD-WR and the WRD_RDY signals are shown in Fig. 2 and other Figures of the present Application are not part of the Utopia protocol. In particular, the event signal is disclosed and claimed. This event signal indicating a status of the buffer memory for both the receive and the transmit modes of operation. For the receive mode, the event signal indicates that the buffer memory unit has a complete data cell stored therein. This data cell can then be appropriately redirected through the direct memory unit. For the transmit mode, the event signal indicates to the direct memory access unit that space is available for the storage of an entire data word. This event signal is not a matter of design choice. By signaling the status of the buffer memory unit, the difference between the performance of the direct memory access unit and the buffer memory unit is compensated for. In other words,

the extremely rapid direct memory access unit is activated only when a complete data cell can be transmitted. This implementation insures that the activity of the direct memory access unit will not be interrupted once a data transfer is begun. Claims 1, 8, and 12, the independent Claims, have been amended to specifically refer to the event signal. In addition to these limitations, Claims 7, 21 (newly added) and Claim 20 describe the clearing of the event signal, the clearing providing an improvement in performance.

Referring now to the Sun reference, this reference also describes a Utopia-protocol interface for asynchronous transmission of data. The thrust of the disclosure is the segmentation and reassembly of variable data cells. Some signals are described in the Sun reference. For example, in the section cited by Examiner, in Col. 3, lines 1-12, a multi-bit address signal (asserting read or write signal), asserting multi-bit data signal and an address signal are described. Notice that in lines 1-3 of Col. 3, the memory interface addresses an external memory in a conventional manner. While it is not completely clear how this exchange is related to the data exchange of the present invention, it appears that nothing extraordinary, i.e., no new signals, such as the event signal, are employed by the Sun reference. Consequently, the rejection of Claims 1 and 3-20 under 35 U.S.C. 102(b) as being anticipated by the Sun reference is respectfully traversed.

In addition, the Claims of the present application include the limitation that the interface unit can act in a master mode or in a slave mode. In certain applications, particularly applications involving digital

signal processors, it is for the interface unit of the present invention to be able to act in either the master mode or the slave mode. The Sun reference does not appear to disclose, teach or suggest this distinction. For this reason also, the rejection of Claims 1 and 3-20 under 35 U.S.C. 102(b) as being anticipated by the Sun reference is respectfully traversed.

Therefore, rejection of Claims 1 and 3-21 under 35 U.S.C. 102(b) as being anticipated by the Sun reference is respectfully traversed. In addition, a possible rejection under 35 U.S.C. 103 as being unpatentable in view of the Sun reference would be traversed because the Sun reference does not include features sought to be protected by the claims of the present Application.

CONCLUSION

In view of the foregoing discussion and the foregoing amendments, it is believed that Claims 1 and 3-21 are now in condition for allowance and allowance of Claims 1 and 3-21 is respectfully requested. Applicants hereby respectfully request a timely Notice of Allowance be issued for this Application.

Respectfully submitted,

William W. Holloway
Attorney for Applicants
Reg. No. 26,182

Texas Instruments Incorporated
PO Box 655474, MS 3999
Dallas, TX 75265
(281) 274-4064